ABSTRACT OF THE DISCLOSURE

A clock multiplication circuit simple in configuration, easy to adjust the characteristics thereof, and capable of shortening lockup time. The circuit delivers an output clock signal at a frequency that is a multiple of the frequency of a reference clock signal as inputted. A counter counts the number of rising edges of the output clock signal existing during a High level period of the reference clock signal, delivering a count value CN. A subtracter subtracts the count value from a reference value BN, delivering a difference value DN. An adder adds the difference value to a preceding integrated value, calculating a new integrated value. A DA converter delivers the analog control voltage corresponding to the integrated value. A VCO delivers the output clock signal at a frequency corresponding to the analog control voltage. The frequency of the output clock signal is controlled such that DN = BN – CN = 0.